CLEAN VERSION OF PENDING CLAIMS

FIELD EMISSION DEVICES HAVING STRUCTURE FOR REDUCED EMITTER TIP TO GATE SPACING
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Claims 36-60, as of November 15, 2001 (Date of Response to First Office Action after RCE)

36. A field emitter array, comprising:

a number of cathodes formed in rows along a substrate;

a gate insulator formed along the substrate and surrounding the cathodes;

a number of gate lines formed on the gate insulator; and

a number of anodes formed in columns orthogonal to and opposing the rows of cathodes, the field emitter array formed by a method comprising:

forming a number of cathode emitter tips in cathode regions of the substrate;

forming a gate insulator layer on the emitter tips and the substrate, wherein

forming the gate insulator layer includes ion etching the insulator layer such that the insulator layer is formed thinner around the emitter tips than in an isolation region of the substrate;

forming a number of gate lines on the gate insulator layer; and

forming a number of anodes opposite the emitter tips, and

wherein a distance separating the number of cathode emitter tips from the number of gates lines is significantly thinner than a separation distance separating the number of gate lines and the substrate.

37. The field emitter array of claim 36, wherein the number of gate lines and the number of cathodes are formed using a self-aligned technique.

38. The field emitter array of claim 36, wherein the number of cathodes include polysilicon cones.

39. The field emitter array of claim 36, wherein the number of cathodes include metal silicides on the polysiiicon cones.

40. The field emitter array of claim 36, wherein the substrate includes glass.

41. The field emitter array of claim 36, wherein the number of gate lines include refractory metals.

42. The field emitter array of claim 36, wherein the number of gate lines include doped polysilicon.

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43. (Amended) A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathodes formed in rows along the substrate;

a gate insulator formed along the substrate and surrounding the cathodes;

a number of gate lines formed on the gate insulator; and

a number of anodes formed in columns orthogonal to and opposing the rows of cathodes, wherein the anodes include multiple phosphors, and wherein the intersection of the rows and columns form pixels, the field emitter array formed by a method comprising:

forming a number of cathode emitter tips in cathode regions of the substrate;

forming a gate insulator layer on the emitter tips and the substrate, wherein forming the gate insulator layer includes ion etching the insulator layer such that the insulator layer is formed thinner around the emitter tips than in an isolation region of the substrate;

forming a number of gate lines on the gate insulator layer; and

forming a number of anodes opposite the emitter tips;

wherein a distance separating the number of cathode emitter tips from the number of

gates lines is significantly thinner than a separation distance separating the number of gate lines and the substrate;

a row decoder and a column decoder each coupled to the field emitter array in order to selectively access the pixels; and

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a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

44. The flat panel display of claim 43, wherein the number of gate lines and the number of cathodes are formed using the self-aligned technique.

45. The flat panel display of claim 43, wherein the number of cathodes include metal silicides on the polysilicon cones.

46. The flat panel display of claim 43, wherein the number of gate lines include refractory metals.

47. (Amended) A field emitter array, comprising:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

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a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathodes.

48. The field emitter array of claim 47, wherein the number of cathodes include polysilicon cones.

49. The field emitter array of claim 47, wherein the number of gate lines include refractory metals.

50. The field emitter array of claim 47, wherein the number of gate lines include doped polysilicon.

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51. (Amended) A field emitter array, comprising:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

C 3 a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathodes;

wherein the number of cathodes include metal silicides on the polysilicon cones.

52. (Amended) A field emitter array, comprising:

a number of cathodes in rows along a semiconductor-on-glass substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathodes.

53. (Amended) A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness;

a number of anodes located in columns orthogonal to and opposing the rows of cathodes; and

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a row decoder and a column decoder each coupled to the field emitter array; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

54. The flat panel display of claim 53, wherein the number of gate lines and the number of cathodes are formed using the self-aligned technique.

55. The flat panel display of claim 53, wherein the number of cathodes include metal silicides on the polysilicon cones.

56. The flat panel display of claim 53, wherein the number of gate lines include refractory metals.

57. (Amended) A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathodes in rows along a substrate;

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a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness;

a number of anodes located in columns orthogonal to and opposing the rows of cathodes, wherein the anodes include multiple phosphors, and wherein the intersection of the rows and columns form pixels; and

a row decoder and a column decoder each coupled to the field emitter array in order to selectively access the pixels; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

58. The flat panel display of claim 57, wherein the number of gate lines and the number of cathodes are formed using the self-aligned technique.

59. The flat panel display of claim 57, wherein the number of cathodes include metal silicides on the polysilicon cones.

60. The flat panel display of claim 57, wherein the number of gate lines include refractory metals.